## AMENDMENTS TO THE SPECIFICATION

Please replace paragraph number **[0030]** with the following rewritten paragraph:

**[0030]** Referring to drawing FIGS. 1A through 1F, the process of manufacturing a packaged semiconductor device according to an embodiment of the present invention is shown. Illustrated in drawing FIG. 1A is a cross-sectional view of a bare substrate 102. The substrate 102 material may include a conventional silicon wafer or other bulk silicon substrate such as is well known in the art. However, it is understood that this substrate 102 may comprise other well-known substrates such as a ceramic or other suitable material. A plurality of cavities 105 is formed in ~~the~~ a top surface (also referred to as an attachment surface) 104 of the substrate 102, such as through a conventional anisotropic silicon etching process. The cavities 105 are each defined by a cavity base 108 and cavity walls 110. As indicated in drawing FIG. 1A, the cavity walls 110 may be formed to exhibit a generally rectangular geometry in cross section such that the cavities 105 are generally cubic in shape. However, the cavities 105 may exhibit other geometries such as, for example, cylindrical, conical, frustoconical, pyramidal, frustopyramidal or semispherical.

Please replace paragraph number **[0035]** with the following rewritten paragraph:

**[0035]** After the molding layer 119 is disposed on the top surface 104 of the substrate 102 and properly cured, a portion of the substrate 102 along its bottom surface 106 is removed as is shown in drawing FIG. 1E. It is noted that, for purposes of clarity, the assembly, as shown in drawing FIG. 1E (as well as in subsequent drawing FIG. 1F), is flipped upside down relative to that which is shown in drawing FIGS. 1A through 1D. The portion of material may be removed from the bottom surface 106 of the substrate 102 by techniques such as back-grinding, abrasive planarization techniques such as chemical-mechanical planarization (CMP), etching or an atmospheric downstream plasma (ADP) process offered by Tru-Si Technologies of Sunnyvale, CA, which is known by those of ordinary skill in the art. Material is removed from the bottom surface 106 of the substrate 102 until the conductive bumps 116 are exposed, creating a new bottom

surface (also referred to as an opposing surface) 106′ of the substrate 102, as shown in FIG. 1E. With the conductive bumps 116 exposed, a system on a chip structure has been created with an array of exposed conductive bumps 116.

Please replace paragraph number **[0038]** with the following rewritten paragraph:

**[0038]** As shown in drawing FIG. 2B, a layer of die attach material 218 is applied in the cavities 205. Discrete semiconductor dice 214 are then placed in the cavities 205 with the active surface 220 of the semiconductor dice 214 facing upwards and the back surface 216 of the semiconductor dice 214 being attached to the base 208 of its respective cavity 205 via the die attach material 218. As shown in drawing FIG. 2C, a first dielectric layer 222 is applied over ~~the~~ a top surface (also referred to as a first surface) 204 of the substrate 202 and which may fill in any gaps 221 between the sides of the semiconductor dice 214 and the cavity walls 210. The first dielectric layer 222 may be applied in a conventional process such as spin coating or spray coating. Finally, as shown in drawing FIG. 2D, a plurality of vias or openings 224 is formed in the first dielectric layer 222, such as by an etching process, thereby exposing the plurality of underlying signal connection devices shown as bond pads 215.